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To : mamatha@research.iiit.ac.in, mamatas2001@yahoo.com

26-Jan-2014

Dear Mrs. Samson:

The above manuscript, entitled "High Data Stability Triple-Threshold-Voltage Seven-Transistor SRAM Cells" with Ms. Zhu as contact author has been submitted to International Journal of Electronics.

I would be grateful if you would kindly agree to act as a reviewer for this paper. The abstract appears at the end of this letter, along with the names of the authors.

Please let me know as soon as possible if you will be able to accept my invitation to review. To do this please either click the appropriate link below to automatically register your reply with our online manuscript submission and review system, or e-mail me with your reply.

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I realise that our expert reviewers greatly contribute to the high standards of the Journal, and I thank you for your present and/or future participation.

Sincerely,
Dr. Alaa Abunjaileh
International Journal of Electronics Associate Editor
ijeditor@leeds.ac.uk

MANUSCRIPT DETAILS

TITLE: High Data Stability Triple-Threshold-Voltage Seven-Transistor SRAM Cells

AUTHORS: Zhu, Hong; Kursun, Volkan

ABSTRACT: Conventional Static Random Access Memory (SRAM) cells suffer from an intrinsic data instability problem due to directly-accessed data storage nodes during a read operation. Noise margins of memory cells further shrink with increasing variability and decreasing supply voltage in scaled CMOS technologies. A selected set of novel seven-transistor (7T) and conventional six-transistor (6T) multi-threshold-voltage memory circuits are characterized for layout area, data stability, write margin, operation speed, active power consumption, and idle mode leakage currents in this paper. A triple-threshold-voltage 7T SRAM cell provides up to 2.2X stronger data stability and 81.5% lower leakage power consumption as compared to traditional 6T SRAM cells in a UMC 80nm CMOS technology.